Smart Grid Synchrophasor Standards and SynchroMetrology Laboratory Support Project

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1 Introduction

This report is "Quarter Two" Report for the Smart Grid Synchrophasor Standards and SynchroMetrology Laboratory Support Project; NIST Contract No. SB1341-10-SE-0958. The Contract requires three quarterly reports and a final report at the completion of the project. Each report includes recommendations to the industry in accordance with NIST objectives.

2 Background

Title XIII of the 2007 Energy Independence and Security Act (EISA) highlights the components of a secure and reliable power supply, together designated as Smart Grid. To emphasize the importance of Smart Grid as a national priority, through the American Reinvestment and Recovery Act (ARRA), the United States Federal Government has made significant investments in Smart Grid programs. This investment includes providing grants for matching funding for 10 projects related to Synchrophasor technology at the total cost of nearly $400 million dollars. Over 847 PMU will be implemented through these programs within 3 years.

A key to the success of this investment is the availability of Smart Grid interoperability standards that reduce the need for customized integration of new equipment and its associated costs, and ensure that devices deployed today will readily work with devices and systems in the existing grid as well those deployed in the future. EISA (section 1305 of Title XIII) tasks NIST with the development of interoperability standards framework to support Smart Grid.

To expedite harmonization of standards and support the activities of PAP12[1] and PAP13[2] , NIST released a public tender[3] for consulting services. NIST outlined a detailed scope of work to accelerate the harmonization between standards for measuring equipment and communication relevant to measurement of grid conditions by Phasor Measurement Units (PMUs) and standards that cover substation automation, transmitting data from field equipment within the substation and beyond. The scope also included support for the further development of the NIST Synchrometrology Laboratory to extend its capabilities to support future communication standards and interoperability testing.

Through competitive procurement, NIST selected ESTA International, LLC (ESTA), an energy strategy and technology advisory firm and its subcontractor Quanta Technology LLC (QT), an energy technology consulting firm, to support this program. The ESTA/QT team and the NIST project team launched the project with a kick-off meeting in October 2010 and will conclude the project in September 2011.

The scope of work covers three specific areas:

[1] PAP 12 – Harmonization and Mapping of IEEE 1815 (DNP Service Profile) and IEC 61850 Standards

[2] PAP 13 – Harmonization of IEEE C37.118 with IEC 61850 and Precision Time Synchronization

[3] Request for Quotation – SB1341-10-RQ-0531 issued on July 27, 2010

A. Further development of the SynchroMetrology testbed for enhanced capabilities, including development of requirements, testing and certification approaches for PMUs and PDCs, testing of protocols in support of SynchroMetrology standards and development of interoperability tests.

B. Harmonization of relevant standards (IEEE C37.118 and IEC 61850, and DNP3.0 and IEC 61850) in support of tasks outlined in Priority Action Plan 12 and Priority Action Plan 13.

C. Development of requirements for Phasor Data Concentrators (PDCs), Phasor Measurement Unit (PMU)-PDC and PDC-PDC communications methods

The deliverable documents for this undertaking consist of three quarterly reports plus a final report, each summarizing the accomplishments during the reporting period. The following tables highlight the tasks, subtasks, and expected timeline for delivery as outlined in the Request for Quotation.

3 Progress during the Reporting Period

The progress for each task is as follows:

3.1 Task 1: SynchroMetrology Testbed Extension Requirement Analysis

Preliminary Recommendations for NIST Testbed Extension was completed and submitted to NIST. A review meeting was held at NIST offices on February 16, 2011. ESTA/Quanta presented an overview of the report and NIST comments were received.

Appendix A contains the Preliminary Recommendations. Final recommendations incorporating NIST comments will be included in the project Final report per schedule.

3.2 Task 2: Support of PAP 12 and PAP 13 Activities

Task 2 focuses on support for two NIST Priority Action Plans – PAP 12 and PAP 13. The ESTA/QT team has actively participated in all PAP 12 and PAP 13 meetings since the start of the project and has become an integral part of these Priority Action Plan working groups. The progress of each PAP is discussed below.

3.2.1 Priority Action Plan 12 (PAP 12)

To expedite PAP 12 activities in order to develop an approved standard for mapping of IEEE 1815 (DNP Project Profile) and IEC 61850 in 2011, considering the IEEE Standards Committee schedule, the activities in PAP12 were modified and Task 2 activities realigned accordingly.

Working closely with PAP 12 members, the ESTA/QT team embarked on a fast track approach of developing the draft IEEE 1815.1 Standard. The ESTA/QT team using the outline previously prepared by the PAP 12 mapping committee developed the draft of the standard in IEEE format. The standard is designated as IEEE 1815.1.

During this period,

a. ESTA/QT team members attended the SGIP Face-to-Face Meeting in Nashville.
b. ESTA/QT team participated in PAP12 regular teleconferences.
c. ESTA/QT project team members participate in Working Group C14.

The ESTA/QT team has continued to support the development of this standard both through participation in PAP12 and IEEE WG C14 activities. ESTA/QT is receiving updates from the C14 Mapping Sub-group and editing the document until completion of the first draft. The target for this activity is to submit it to the IEEE Review Committee in July 2011. The IEEE C14 Working Group aims to obtain approval from IEEE and afterwards, possibly seek approval by the IEC (as IEC 61850-80-2)

Appendix B contains the table of contents of the latest version of the IEEE 1815.1 document.

3.2.2 Priority Action Plan 13 (PAP 13)

The ESTA/QT team has members active in PSRC Working Group 14 responsible of C37.118.2 and IEC TC57 Working Group 10 responsible for IEC61850-90-5 and as such is intimately familiar with the developments. The team has provided recommendations for harmonization of IEC 61850 and IEEE C37.118, including text, diagrams, and models as input to IEC WG 10 for the draft mapping document IEC 61850-90-5, in support of PAP13 tasks.

During this period,

a. ESTA/QT team members attended the SGIP Face-to-Face Meeting in Nashville.
b. ESTA/QT team participated in regular PAP13 teleconference calls.
c. ESTA/QT team provided recommendations for PAP 13 for harmonization of IEEE C37.118 with IEC 61850.

Appendix C provides ESTA/QT recommendations.

3.3 Task 3: Requirements, Testing and Certification Approaches for PMUs and PDCs

During this reporting period, the ESTA/QT has actively supported the NASPI Performance and Standards Task Team (PSTT) by participation at the NASPI February 2011 Meeting in Fort Worth TX and through participation at monthly PSTT meetings. The ESTA/QT has provided NASPI with:

- Recommendations for methods for PMU-PDC/PDC-PDC communications as input to the NASPI PSTT
- Recommendations for PDC testing and certification approaches as input to the NASPI PSTT

Appendix D contains the ESTA/QT recommendations for PMU-PDC/PDC-PDC communications and ESTA/QT recommendations for PDC Testing and Certification.

Appendix A. SynchroMetrology Testbed Extension Requirements

The ESTA/QT Preliminary Recommendations for the Testbed extension are documented in the following sections.

NIST Synchrophasor Standards and SynchroMetrology Lab Support Project Report

Preliminary Recommendations for NIST Testbed Extension

Prepared by:
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Executive summary

This document presents preliminary recommendations from the project team to NIST for further development of the SynchroMetrology testbed for enhanced capabilities, including development of requirements, testing and certification approaches for PMUs and PDCs, testing of protocols in support of SynchroMetrology standards and development of interoperability tests.

The document reviewed and summarized the current capabilities of NIST SynchroMetrology testbed, the industry needs for additional testing and calibration, and various activities and projects in synchrophasor standard development and testing related areas.

Based on these reviews, the project team has concluded that

- There is a clear need for NIST to take immediate action to further enhance and develop its testbed to support SGIG projects and other synchrophasor deployment projects
- There are two identified areas that need NIST's urgent action to develop test procedures and test & calibration capabilities from NIST existing testbed and other test facilities
    - Full IEEE C37.118.1 compliance test and calibration
    - GPS clock testing and certification
- There are three other areas that need NIST to closely follow with the various standard / guideline development activities on a regular basis and take appropriate actions when the time is ready
    - IEEE 1588 compliance test
    - IEEE C37.118.2 and IEC 61850-90-5 compliance test
    - PDC testing and calibration

The project team recommends that NIST, after its review of this document, provides guidance to project team for taking proper actions to support NIST in developing test procedures and plans in NIST selected areas.

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1 About this document

This document presents preliminary recommendations from the project team to NIST for further development of the SynchroMetrology testbed for enhanced capabilities, including development of requirements, testing and certification approaches for PMUs and PDCs, testing of protocols in support of SynchroMetrology standards and development of interoperability tests.

This document is delivered as "Appendix A – Preliminary recommendations for NIST Testbed Extension" of Quarter 2 report.

The document is organized as follows:

- Section 1: (This section) provides a summary description about this document and the organization of the document.
- Section 2: Provides a summary of the current capabilities of the NIST testbed.
- Section 3: Presents the identified industry needs and a summary of related standards development activities that require the further development of the NIST testbed
- Section 4: Identifies areas of the NIST testbed for further development
- Section 5: Conclusions and recommendations

2 Summary of NIST Testbed current capabilities

The table below summarizes the current test capabilities of the NIST test systems as of December 1, 2010. NIST testing systems were developed based on the current Standard C37.118-2005 and NASPI's "PMU System Testing and Calibration Guide" published in December 2007. Table numbers below refer to Tables of IEEE Standard C37.118-2005.

Table 1 shows that NIST does a good job of covering all requirements for the synchrophasor standard developed in 2005 and some additional dynamic and unbalanced tests. However, this standard is being updated and will be republished in early 2011 with significant requirement changes not covered by current NIST testing. Numerous electric utilities and PMU manufacturers will need to know how well the PMUs perform relative to the new standard as described below in section 3. Section 4 shows a table similar to Table 1 of the updates needed to the NIST test system to cover the requirements of the new standard.

Table 1 Current NIST PMU Test Capabilities

Requirement	Currently tested by NIST	Changes needed for NIST?	Type of change to meet current standard	Difficulty of testing changes	Difficulty of analysis changes
C37.118-2005 Table 1. Reporting rates					
Basic Functionality	Yes	No	None	None	None
Reporting Rates	Yes	No	None	None	None
C37.118-2005 Table 3. Steady -State Phasor Requirements					
Signal Frequency	Yes	No	None	None	None
Signal Magnitude Voltage	Yes	No	None	None	None
Signal Magnitude Current	Yes	No	None	None	None
Phase Angle	Yes	No	None	None	None
Harmonic Distortion	Yes	No	None	None	None
Out-of-Band Interference	Yes	No	None	None	None
C37.118-2005 Tables 4. - 6. Time Quality Bits					
Proper Time Quality Indication	Yes	No	None	None	None

Requirement	Currently tested by NIST	Changes needed for NIST?	Type of change to meet current standard	Difficulty of testing changes	Difficulty of analysis changes
C37.118-2005 Tables 7. - 13. Message Formats					
Commands	Yes	No	None	None	None
Message Formats	Yes	No	None	None	None
None IEEE C37.118-2005 Tests					
Unbalanced three phase					
Unbalanced Phase	Yes	No	None	None	None
Unbalanced Amplitude	Yes	No	None	None	None
Phasor Bandwidth Requirements with modulated signals					
Amplitude Modulation	Yes	No	None	None	None
Phase Modulation	Yes	No	None	None	None
Phasor Requirements with Step Changes					
Amplitude	Yes	No	None	None	None
Phase	Yes	No	None	None	None
Frequency	Yes	No	None	None	None

NIST PMU testing is presently done on two test systems. The NIST Steady-state test system is used to perform the tests in the first five groups above, the reporting rates, the steady-state phasor requirements, the time quality bits, the message formats, and the unbalance three-phase tests. The NIST Dynamic test system us used to perform the tests in the last two groups of tests, the phasor bandwidth requirements with modulated signals and the phasor requirements with step changes tests.

3 Overview of the needs for further development

There is a clear need for NIST to further develop its SynchroMetrology testbed. The urgent needs come directly from the SGIG synchrophasor projects with US government ARRA matching funding and a number of other synchrophasor projects funded by utilities' own funding. The needs for interoperability standards for these projects have accelerated the development of a number of standards. The following summarizes these needs.

3.1 Industry needs

3.1.1 Synchrophasor technology and wide-area situation awareness

Synchrophasor technology has been recognized by the industry as the key enabling technology for wide-area monitoring, protection, automation and control system (WAMPACS). The technology is the foundation for achieving advanced wide-area situation awareness (WASA) for preventing large scale power system failures such as the one which occurred in the August 14, 2003. WASA is considered to be one of the priority areas in the overall Smart Grid implementation in US.

To enable effective wide-area situation awareness, various WAMPACS must be implemented by their respective entities and interconnect with each other to exchange measurement data and other messages within and among these WAMPACS.

Global performance of measurement devices is critical for wide-area situation awareness. All sensors from various vendors and installed for these systems must be able to produce consistent and comparable results in order for these systems to work properly.

Various components of these systems from different vendors must use and properly implement the same communication protocols to be able to exchange data and other messages with each other.

3.1.2 Current and future synchrophasor projects

As part of the smart grid stimulus funding, ten smart grid investment grant funded synchrophasor projects have been awarded by DOE. The total investment of these projects including about $200 million DOE matching funds and awardees own funding is about $400 million.

In addition, there are many on-going and planned synchrophasor projects fully funded by their respective entities' own capital investment.

It is expected that synchrophasor technology will become more commonplace and substantial investment will be made in next few years.

Most of these projects have included the PMU and PDC testing and certification as part of their project quality assurance, in order to ensure that all PMUs and PDC procured and deployed for their systems are compliant to industry synchrophasor standards and are interoperable with each other.

For many of these projects, particularly the DOE SGIG synchrophasor projects with fixed three-year project duration, there is an urgent need to immediately start these testing activities in order to meet their respective project schedules and plans.

3.1.3 NIST and its framework for Smart Grid interoperability standards

Under the Energy Independence and Security Act (EISA) of 2007, the National Institute of Standards and Technology (NIST) is assigned "*primary responsibility to coordinate development of a framework that includes protocols and model standards for information management to achieve interoperability of Smart Grid devices and systems…"* [EISA Title XIII, Section 1305].

To carry out its EISA-assigned responsibilities, NIST has devised a three-phase plan to rapidly identify an initial set of standards, while providing a robust process for continued development and implementation of standards as needs and opportunities arise and as technology advances. The plan is described in its "NIST Framework and Roadmap for Smart Grid Interoperability Standards, Release 1.0" as

1. **Engage stakeholders in a participatory public process to identify applicable standards and requirements, and gaps in currently available standards, and priorities for additional standardization activities.** With the support of outside technical experts working under contract, NIST has compiled and incorporated stakeholder inputs from three public workshops, as well as technical contributions from technical working groups and a cyber security coordination task group, into the NIST-coordinated standards-roadmap effort.

2. **Establish a Smart Grid Interoperability Panel forum to drive longer-term progress.** A representative, reliable, and responsive organizational forum is needed to sustain continued development of interoperability standards. On November 19, 2009, a Smart Grid Interoperability Panel was launched to serve this function.

3. **Develop and implement a framework for conformity testing and certification.** Testing and certification of how standards are implemented in Smart Grid devices, systems, and processes are essential to ensure interoperability and security under realistic operating conditions. NIST, in consultation with stakeholders, plans to develop an overall framework for testing and certification, with initial steps completed by early 2010.

Developing enhanced testing and calibration capabilities for synchrophasor technology at NIST is an important part of supporting the industry in implementing the framework for conformity testing and certification. NIST will need to provide the traceability of many smart grid interoperability standards to national and international standards that they derived from.

3.2 Synchrophasor related standard development activities summary

There are a number of standard development activities that are relevant to both ARRA funded SGIG synchrophasor and utilities funded synchrophasor projects.

The definition of standard used in this document includes standards, reports, and guidelines developed and published by Standard Development Organizations (SDO), user groups, and various industry organizations.

3.2.1 IEEE C37.118

The IEEE C37.118-2005 is currently being revised. The standard has been broken into two standards. C37.118.1 will contain the performance requirements for PMUs and C37.118.2 will contain the data communication and messaging requirements for PMUs and PDCs.

C37.118.1 is being revised by Power System Relaying Committee (PSRC) Working Group (WG) H11. The main thrust of this revision is to add dynamic test requirements for PMUs and to include the testing of the frequency and rate-of-change-of-frequency (ROCOF) that is reported as part of the PMU data. The details of these additions and the effects that they have on the NIST test system are outlined below in the section 4.1 (Main areas identified for further development) IEEE C37.118.1 test.

C37.118.2 is being revised by PSRC WG H19. For backward compatibility with C37.118-2005, this working group is working under the premise of minimizing the changes to this standard from existing C37.118-2005 standard. The main change being discussed currently is the addition of a new Configuration 3 message that allows for more information about the PMU and the phasors being calculated to be sent from the PMU.

3.2.2 IEC 61850

IEC TC57 WG10 is current developing a standard for synchrophasors as IEC 61850-90-5. The draft standard has been developed and is currently under review and comments. It intends to address the cyber security aspect as an integral part of the finalized standard, which is currently under development. Once completed and published by IEC, the objective is to dual-logo the standard by IEEE to harmonize the synchrophasor communication protocol.

3.2.3 Harmonization between IEEE C37.118 and IEC 61850

IEEE and IEC plan to harmonize the synchrophasor related standards developed by each organization. The decision to split IEEE C37.118-2005 into two standards, C37.118.1 for measurement performance requirement and C37.118.2 for communication protocols is to help facilitate the harmonization, as IEC 61850 standard deals with communication protocols only.

The current plan is to publish IEEE C37.118.1 and to dual logo it to become an IEC standard. IEEE C37.118-2005 and the C37.118.2 will continue to serve the current needs. IEC 61850-90-5, once published, is intended to be dual logo to also become an IEEE standard.

3.2.4 IEEE 1588

PSRC WG H7/Sub C7 under Galina Antonova has developed a Power Profile for the IEEE Std 1588 Precision time Protocol Standard. This Standard, to be published as IEEE C37.238, will standardize the use of IEEE 1588 in power system substations for the use of synchronizing instruments to UTC. This approach

is expected to replace the use of multiple GPS clocks in substations and the need to transmit timing data over IRIG-B connections between the clocks and PMUs and other instruments.

NIST and the University of Michigan have developed testbeds for IEEE Std 1588 to help determine the expected uncertainty of devices with this capability under conditions typical in substations. Two publications on these developments were recently published at the ISPCS conference held September 29 to October 1, 2010 at the University of New Hampshire. One paper was titled "An IEEE 1588 Time Synchronization Testbed for Assessing Power Distribution Requirements." The other paper was titled "Using clock accuracy to guide model synthesis in distributed systems: An application in power grid control."

The NIST test system has obtained a 1588 compatible card for the Dynamic PMU test system. NIST is starting to explore the application of this to testing PMUs.

3.3 Other synchrophasor test related projects and activities

There are several projects and activities related to PMU / PDC testing and calibration that are currently underway. These projects and activities are summarized below.

3.3.1 PSRC C5 WG

PSRC WG C5 is currently working on developing a "Guide for synchronization, calibration, testing and installations of PMU for power system protection and control" (PC37.242). The guide being developed is based on the previously published NASPI PSTT documents / guides with necessary updates and addition to reflect the latest development of the synchrophasor standards and to address the needs of intended users. The guide is intended to be used by power system protection professionals for PMU installation and covers the requirements for synchronization of field devices and connection to other devices including phasor data concentrators.

The guide addresses the following areas:

- Considerations for the installation of PMU devices based on application requirements and typical bus configurations
- Techniques focusing on the overall accuracy and availability of the time synchronization system
- Test and calibration procedures for phasor measurement units (PMUs) for laboratory and field applications
- Communication testing for connecting PMUs to other devices including Phasor Data Concentrators (PDC)

The test and calibration procedures for phasor measurement units (PMUs) for laboratory and field applications part is based on the NASPI PSTT previously published "PMU System Testing and Calibration

Guide" that has been updated by Gerard Stenbakken, Ken Martin, and Allen Goldstein to reflect the latest development of the PC37.118.1 synchrophasor standard.

3.3.2 NASPI PSTT activities

There are a number of priority activities that currently are underway within the NASPI PSTT. These activities are carried out with urgency in order to support the industry and the SGIG projects. These activities are as follows:

- **Define certification process for PMUs** – PSTT is developing a white paper on PMU certification procedures. The white paper will be based on the NASPI PSTT "PMU System Testing and Calibration Guide" that has been updated in anticipation of new IEEE C37.118.1 standard publication, and to be included in IEEE PC37.242.

- **Phasor data concentrator requirements** – Current synchrophasor standards and the standards under development are primarily for PMU performance requirements and synchrophasor data transfer protocols. PSTT is developing a document for PDC's functional and performance requirements of the main PDC functions.

- **PMU-PDC/PDC-PDC communication methods** – PSTT is developing a guide for additional communication methods to address a number of data management, system management, and other functions of a synchrophasor system. The guide will supplement the synchrophasor standards and aims to be integrated into the standards in the future.

- **Phasor data concentrator test and verification standard** – PSTT is also developing a PDC test guideline to provide a standardized way for testing PDCs on the market. The guideline will be developed based on the PDC requirements document.

- **Integration of IEC 61850 and IEEE C37.118** – As has been mentioned above, both IEEE and IEC WGs are working towards the harmonization of the synchrophasor standards published / developed by these WGs. The synchrophasor communication protocol of C37.118 is to be harmonized with IEC 61850. PSTT intends to support the effort and developing recommendations and guideline for facilitating the integration and harmonization of the two standards.

3.3.3 Fluke PMU calibrator development project

Fluke was awarded a grant from NIST to develop a PMU calibration system. They have hired several contractors to do the development of the control software and design concepts. The main part of the hardware will be based on the Fluke 6105A power simulator. Fluke is scheduled to have a prototype ready for some testing and calibration at NIST in the spring of 2011.

3.3.4 Virginia Tech Synchrophasor testing lab

Virginia Tech (VT) is developing a PMU testing and calibration system based on the design of the NIST Dynamic calibration system. The development of VT lab is part of its commitment in performing PMU and PDC testing and certification to PJM's SGIG synchrophasor project. The PJM SGIG project requires VT to complete its lab development by the end of 2010, and starts PMU and PDC calibration and testing in January 2011.

One part of the lab development plan is to calibrate the developed system with NIST system to establish traceability of the VT testing system.

VT has acquired the hardware for the system and has a copy of the NIST software. They are learning to operate the hardware and software and what modifications will be needed to perform all of the tests on the dynamic system. The tests that are performed on the NIST Steady-State test system will need to be modified to operate on the VT test system.

VT has had two teleconferences with Jerry Stenbakken at NIST and visited on December 13-14, 2010. The status of the VT test system is that it may be able to perform some tests in January 2011 and have traceability to NIST in the first quarter of 2011 for most or all of C37.118-2005 tests. After that they will be able to perform these tests for PJM.

3.3.5 GPA PDC test bench

Grid Protection Alliance (GPA) is under a NERC contract to develop an open-source PDC test bench for the industry. It is intended to be developed to provide a base testing platform for generating testing data and capturing PDC output for test and analysis. It is expected that users should be able to add enhanced testing capabilities to the platform.

The BETA version of the test bench is current available from the GPA. GPA will continue its development until the project complete.

4 Main areas identified for further development

Based on the current NIST testbed's capabilities, the industry needs, and the various activities within the industry, we have identified a number of areas that NIST's current testbed will need to be further enhanced and developed to provide adequate support to the industry and the SGIG projects. Some of these enhancement and development will need to be completed in a short time period in order to support the SGIG and other synchrophasor deployment projects.

4.1 Full IEEE C37.118.1 test

Although the IEEE C37.118.1 has not been published yet, the change to its current draft is expected to be minimal before its expected target publishing time frame in mid 2011. There are several areas that the current NIST testbed needs further enhancement and development to support the testing and calibration of PMUs and other PMU calibration systems in accordance with the C37.118.1 standard.

- Dynamic performance tests – although NIST current testbeds have implemented a number of dynamic tests, the new standard has added many more items that will require further development of the testbeds.

- Frequency and the rate-of-change of frequency related tests – the new standard has added tests for these two measurement data. The current NIST testbeds do not have these tests implemented.

- P and M class tests – the new standard defines two classes of performance: P and M classes. Current test process and procedure are geared more toward the M class performance tests. New test processes and procedures should be developed to properly test and calibrate PMUs for P class performance.

Below is a table showing the changes needed to the NIST calibration systems to accommodate the testing required for the proposed revision of the IEEE C37.118.1. This table is based on PC37.118.1 Draft 1.6a and PC37.118.2 Draft 0.9a received Oct 22, 2010. The new standard requirements apply to all phasors not just the positive sequence. This will require changes to all NIST tests in the analysis section. This overall change is significant for the analysis phase.

Table 2 Changes to NIST testing systems because of Proposed Standard Revisions C37.118.1 -2011 and C37.118.2-2011

New Req C37.118.1 or C37. 118.2?	Requirement	Currently tested by NIST	Changes needed for NIST?	Type of change	Difficulty of testing changes	Difficulty of analysis changes
C37.118.1-2011 Table 1. Reporting rates						

New Req C37.118.1 or C37. 118.2?	Requirement	Currently tested by NIST	Changes needed for NIST?	Type of change	Difficulty of testing changes	Difficulty of analysis changes
Per C37.242 perform Out-of-band interference at each reporting rate as part of basic functionality testing. Currently NIST does reduced resolution frequency test.						
No	Basic functionality	Yes	Yes	Change test	Moderate	Moderate
No	Reporting Rates	Yes	Yes, new rates	100 and 120 fps recommended	Significant	Moderate
C37.118.1-2011 Table 3. Steady -State Phasor Requirements						
No	Signal Frequency	Yes	Some	Freq range changes per RR	Slight	Slight
Yes	Signal Frequency Temperature tests	No	Yes	Frequency tests to run at three temperatures	Significant	Slight
No	Signal Magnitude Voltage	Yes	No	None	None	None
No	Signal Magnitude Current	Yes	Yes	Current test to higher value	Slight, Must do on Steady state system	Slight, cannot do all voltages and currents together
No	Phase angle	Yes	No	None	None	None
No	Harmonic Distortion	Yes	No	None	None	None
No	Out-of-Band Interference	Yes	Yes	Interference must be positive sequence and at off nominal freq	Significant, do on Dynamic System	Slight
C37.118.1-2011 Table 4. Steady-state Frequency and ROCOF Requirements						
Yes	Signal Frequency	No	Yes	New test	Moderate	Moderate
Yes	Harmonic Distortion	No	Yes	New test	Moderate	Moderate

New Req C37.118.1 or C37. 118.2?	Requirement	Currently tested by NIST	Changes needed for NIST?	Type of change	Difficulty of testing changes	Difficulty of analysis changes
Yes	Out-of-Band Interference	No	Yes	New test	Moderate	Moderate
C37.118.1-2011 Table 5. Phasor Bandwidth Requirements with modulated signals						
Yes	Amplitude and Phase modulation	Yes	Yes	Limit based on Maximum TVE versus average	Slight	Moderate
Yes	Phase modulation	Yes	Yes	Limit based on Maximum TVE versus average	Slight	Moderate
C37.118.1-2011 Table 6. Frequency and ROCOF Requirements with modulated signals						
Yes	Amplitude and Phase modulation	No	Yes	New test	Significant	Significant
Yes	Phase modulation	No	Yes	New test	Significant	Significant
C37.118.1-2011 Table 7. Phasors Requirements with Frequency Ramp						
Yes	Linear Ramp	No	Yes	New test	Significant	Significant
Yes	Ramp plus 3rd Harmonic	No	Yes	New test	Significant	Significant
C37.118.1-2011 Table 8. Frequency and ROCOF Requirements with Frequency Ramp						
Yes	Linear Ramp	No	Yes	New test	Significant	Significant
Yes	Ramp plus 3rd Harmonic	No	Yes	New test	Significant	Significant
C37.118.1-2011 Table 9. Phasor Requirements with Step Changes						
Yes	Amplitude	Partial	Yes	New test	Significant	Significant
Yes	Phase	Partial	Yes	New test	Significant	Significant
C37.118.1-2011 Table 10. Frequency and ROCOF Requirements with Step Changes						
Yes	Amplitude	Partial	Yes	New test	Significant	Significant
Yes	Phase	Partial	Yes	New test	Significant	Significant

New Req C37.118.1 or C37. 118.2?	Requirement	Currently tested by NIST	Changes needed for NIST?	Type of change	Difficulty of testing changes	Difficulty of analysis changes
C37.118.1 -2011 Section 5.5.7. Reporting Latency						
Yes	Reporting Latency	No	Yes	New test	Significant	Significant
C37.118.2-2011 Tables 4. - 6. Time Quality Bits						
No	Proper Time Quality Indication	Yes	No	None	None	None
C37.118.2-2011 Tables 7. - 13. Message Formats						
No	Commands	Yes	No	None	None	None
No	Message Formats	Yes	No	None	None	None
None IEEE C37.118.1 or C37.118.2 Tests						
Unbalanced three phase						
No	Unbalanced Phase	Yes	No	None	None	None
No	Unbalanced Amplitude	Yes	No	None	None	None

It is estimated, assuming there is adequate funding and resources, the time to complete all of the changes to NIST current test system will be about one year.

As mentioned before, PJM and possibly WECC/PG&E SGIG projects are depended on VT to timely complete the VT test lab development and the lab be calibrated with NIST to establish the traceability. Fluke project will also need NIST to provide the calibration for their developed system in 2011. Without these further enhancement and development, NIST will not be able to provide the full C37.118.1 standard compliancy testing and calibration for both VT lab and Fluke system. The PMU testing by the VT and Fluke systems will be limited to only the tests that can be traceable to the NIST current test systems.

To the extent that these systems are calibrated by the exchange of a PMU or can be programmed to act like a PMU, this will require minimal changes to the NIST system. If these systems are to be calibrated without

sending out a C37.118 format message, then significant changes will be needed in the NIST calibration system to adapt to this configuration, or a more elaborated / complex calibration process / procedure will need to be developed to calibrate each test system.

4.2 GPS clock test and calibration

GPS clock is currently used as a primary timing source to provide accurate UTC traceable clock to PMUs. Based on NIST previous testing experience with various GPS clocks, it is clear that GPS clocks by different vendors have diverse performance characteristics in terms of sensitivity, stability and so on. NIST had one experience of having one GPS clock of the PMUs being tested for the Brazilian grid operators (ONS) certification project not being compatible with the one used by NIST test system. The interfaces of GPS clocks to PMUs are also not uniform from product to product, and some do not provide necessary signaling to PMUs to support the proper implementation of the C37.118 standard for time quality marking.

There is also an issue of compatibility of GPS clocks and PMUs with respect to the drive current needed to communicate with PMUs. Not all GPS clocks can drive some PMUs. Thus, some measure of GPS output drive and PMU input impedance would be useful.

Since GPS clocks play a vital role in the current synchrophasor systems, it would be extremely important to have various GPS clocks being calibrated, and tested for sensitivity and stability, as well as to identify whether the interface of a GPS clock will be able to support a PMU to implement the standard required time quality marking. This information would be very useful for utilities planning GPS clock installations and the reliability of the synchrophasor systems. This problem may lessen as more utilities progress to adopt the use of IEEE 1588 standard for network based accurate timing source distribution. However, since there are no PMUs available today that are 1588 compatible, this change is expected to take several years at least. Even after 1588 is adopted, GPS clocks may still be used as the master timing sources for a synchrophasor system using 1588 network distributed timing sources.

Although NIST already has facility to perform calibration on a GPS clock when it is locked to the satellite signals, new procedures need to be developed to calibrate and certify a GPS clock for sensitivity and stability. Proper identification of the GPS clock interface, whether it is compatible to PMU and support standard required time quality marking, should also be verified and certified.

As a large number of GPS clocks will be purchased and installed along with PMUs and PDCs for SGIG and other synchrophasor projects, this testing and certification capability should be developed by NIST within a very short time period.

4.3 IEEE 1588 test

The NIST test system has obtained a 1588 compatible card for the Dynamic PMU test system. NIST is starting to explore the application of this to test future PMUs that may use 1588 as its primary timing source.

However, since no PMU product, based on our knowledge, that is currently supporting 1588, the need to establish the test capability for PMUs using 1588 is considered as not as urgent as other areas at this

moment. However, NIST testbed should start to make plans to establish this capability, and be ready when PMU products supporting 1588 become available.

4.4 IEEE C37.118.2 and IEC 61850-90-5 test

Both IEEE C37.118.2 and IEC 61850-90-5 are expected to be published in 2011 (or 2012 the latest). Once they become available, it is expected that PMU products supporting both will become available soon. Thus, there will be a need to test and calibrate PMUs that implement these two new standards.

However, both standards developments are not close to their final form yet, thus at this stage, it is difficult to start preparation and estimate the efforts needed for such implementation in NIST testbed.

Tracking the development of both standards, and having a preliminary plan to implement both standards once they are published, are needed for NIST at this stage.

4.5 PDC test and calibration

As PDC requirements document and PMU-PDC/PDC-PDC communication methods are still under the development by NASPI PSTT, and the PDC test guideline is yet to be developed by PSTT at this moment, it is not possible for NIST to start planning and preparing to support PDC test and calibration at this moment.

However, since NIST is directly supporting PSTT in the above three activities, NIST should be ready to start the PDC test and calibration planning and preparation immediately once PSTT completes its tasks.

4.6 Recommended NIST action plans

In view of the above situation, it is highly recommended that NIST make immediate plans and appropriate funding for the following two areas:

- Full C37.118.1 test and calibration capability
- GPS clock test and certification

The development work in these two areas should be started on an ASAP basis in order to be able to support the current SGIG and other synchrophasor deployment projects.

For other areas discussed in this section, it is recommended that NIST should regularly review the progress and status of these activities on a monthly basis and initiate any actions as appropriate.

5 Conclusions and recommendations

The followings are main conclusions and recommendations:

- There is a clear need for NIST to take immediate action to further enhance and develop its testbed to support SGIG projects and other synchrophasor deployment projects
- There are two identified areas that need NIST's urgent action to develop test procedures and test & calibration capabilities from NIST existing testbed and other test facilities
    - Full IEEE C37.118.1 compliance test and calibration
    - GPS clock testing and certification
- There are three other areas that need NIST to closely follow with the various standard / guideline development activities on a regular basis and take appropriate actions when the time is ready
    - IEEE 1588 compliance test
    - IEEE C37.118.2 and IEC 61850-90-5 compliance test
    - PDC testing and calibration

The project team recommends that NIST, after its review of this document, provides guidance to project team for taking proper actions to support NIST in developing test procedures and plans in NIST selected areas.

6 References

[1] IEEE C37.118-2005, "IEEE Standard for Synchrophasors for Power Systems", IEEE 2006

[2] IEEE PC37.118.1 January 2011 Draft

[3] IEEE PC37.118.2 January 2011 Draft

[4] IEEE P1815.1 (future IEC 61850-80-2) January 2011 Draft

[5] IEC 61850-90-5 January 2011 Draft

Appendix B. PAP 12 Support –IEEE 1815.1 Development

ESTA/QT has actively supported PAP12 and IEEE WG C14 for the development of IEEE standard 1815.1 This standard is under review and not approved as of this report date. Below is the table of contents of this standard as of April 2011. As the standard is evolving the whole document is not included in this report.

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Appendix C. PAP 13 Support – Recommendations for Synchrophasor Message Types and Object Modeling

The ESTA/QT team provided recommendations and contributions to Synchrophasor message types and Object Modeling of Synchrophasor Based Devices System Hierarchy in support of PAP 13 as follows:

Synchrophasor Message Types

Type 8 - Calculated data messages ("Synchronized Measurements")

This message type includes the output data from synchronized measuring devices independent from the calculation and synchronization methods. The data will consist of continuous streams of synchronized measurements from each IED, interleaved with data from other IEDs.

Transfer time means for the stream of synchronized measurements a constant delay resulting in a delay for the functions using the measurements (e.g. for protection, visualization or other). Therefore, this transfer time shall be dependent on the requirements of the application. For protection applications it should be small, so no negative impact on an application function is experienced.

Performance class	Requirement	Transfer Time Class	Transfer Time	Typical for Interface (IF)
P13	Delay acceptable for protection functions using the measurements in the substation	TT6	< 3 ms	IF8
P14	Delay acceptable for other functions using the measurements in the substation	TT5	< 10 ms	IF8
P15	Delay acceptable for protection functions using the measurements between substations	TT6	< 3 ms	IF11
P16	Delay acceptable for other functions using the measurements between substations	TT5	< 10 ms	IF11

Object Modeling of Synchrophasor Based Devices System Hierarchy

Protection, monitoring and control systems that use synchrophasors are complex hierarchical systems with PMUs at the bottom of the hierarchy, and PDCs at the different levels of the hierarchy as shown in Figure 1.

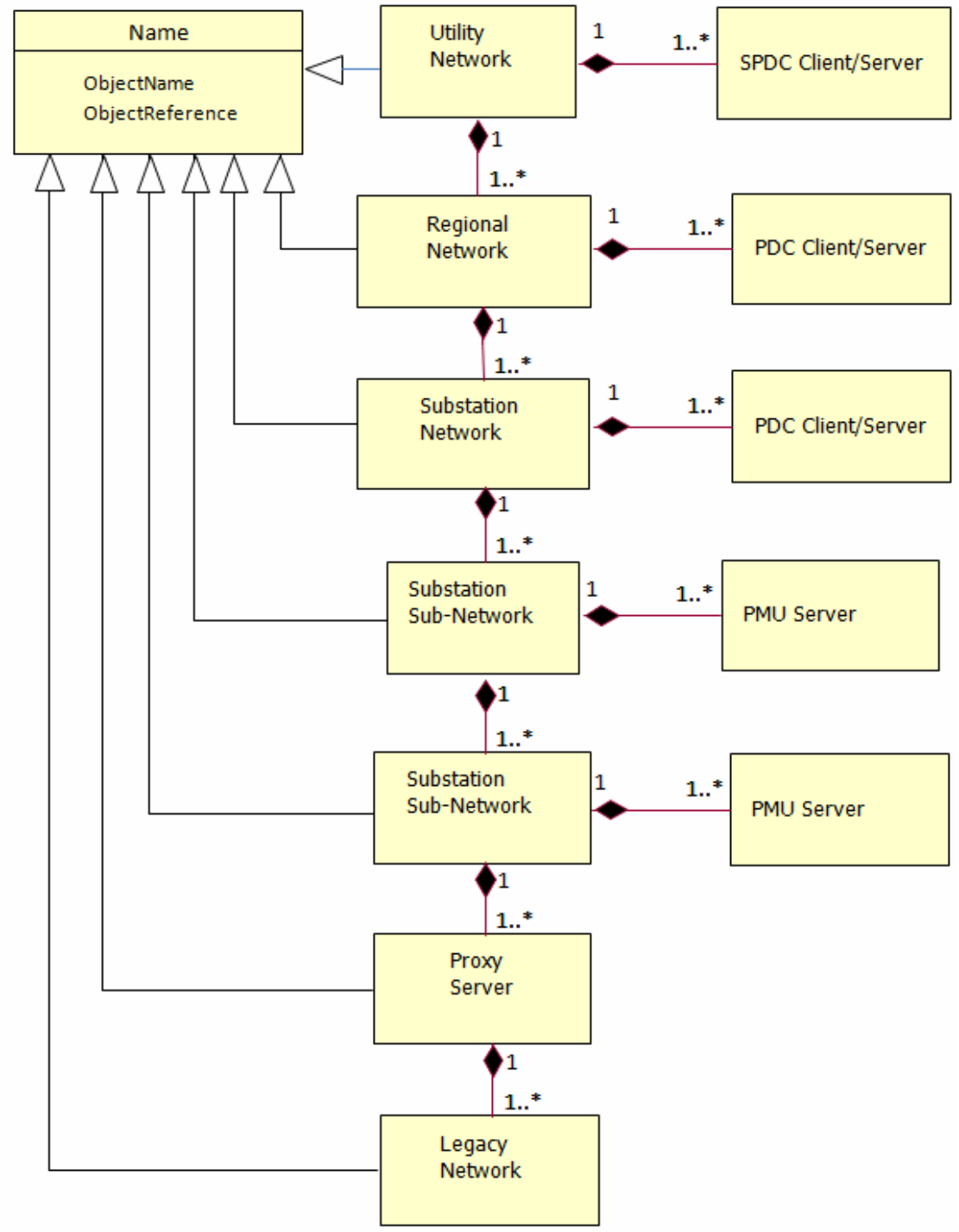

Fig. 1 System hierarchy

PMU Model

The PMU is a function within an IED which is responsible for the calculation and publishing of synchrophasor measurements as defined in IEEE C37.118.
These calculations are based on sampled values produced by the analog input module within the IED containing the PMU function or based on streaming sampled values produced by one or more merging units in the substation that the IED containing the PMU function is subscribing to.

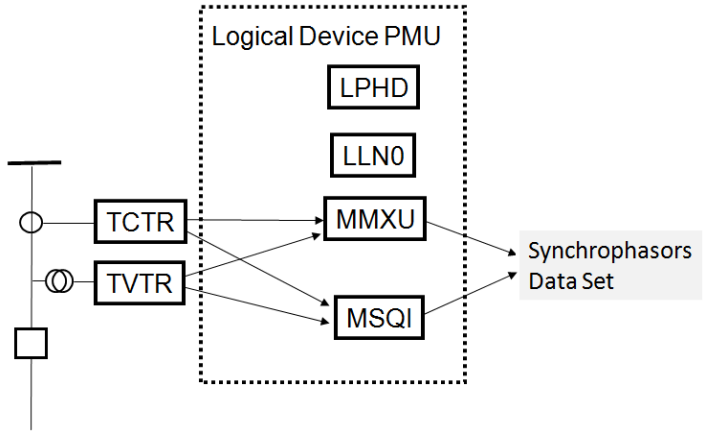

Fig. 2 PMU object model

If the PMU is publishing phase currents and voltages, one or more instances of MMXU will be used.
If the PMU is publishing sequence currents and voltages, one or more instances of MSQI will be used.

Substation PDC Model

The substation Phasor Data Concentrator (PDC) is a function that receives over the substation LAN data from multiple PMUs in the substation. The received data is sorted by their time-tags and provided to other applications to use them. If necessary the PDC may need to perform re-sampling in order to align measurements from devices using different publishing rates.

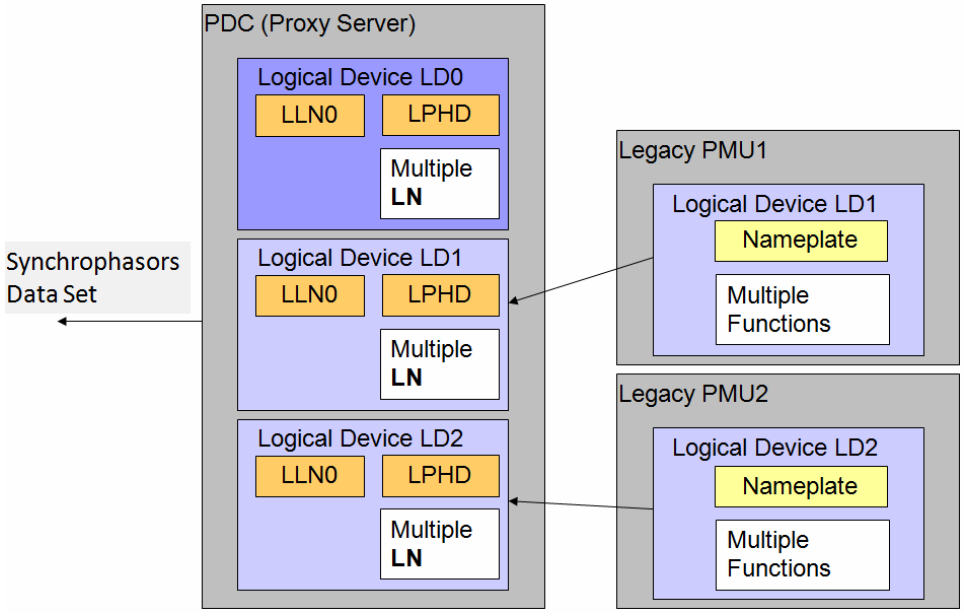

Fig. 3 Substation PDC model with legacy PMUs

A data set containing a representative set of data as required by the upper levels of the system hierarchy is created and published over a wide area interface using UDP multicast.

It is recommended to model the PDC function as a PDC logical device with the Proxy data object in logical node LPHD *Proxy* set to *True*.

The PDC model is based on the nesting of logical devices defined in Edition 2 of IEC 61850.

Regional or System Level PDC

The Regional level Phasor Data Concentrator (PDC) is a function that receives over the wide area network data from multiple PDCs in different substations. The received data is sorted by their time-tags and provided to other applications to use them. If necessary the PDC may need to perform re-sampling in order to align measurements from devices using different publishing rates.

A data set containing a representative set of data as required by the upper levels of the system hierarchy is created and published over a wide area interface using UDP multicast.

It is recommended to model the PDC function as a PDC logical device with the Proxy data object in logical node LPHD *Proxy* set to *True*.

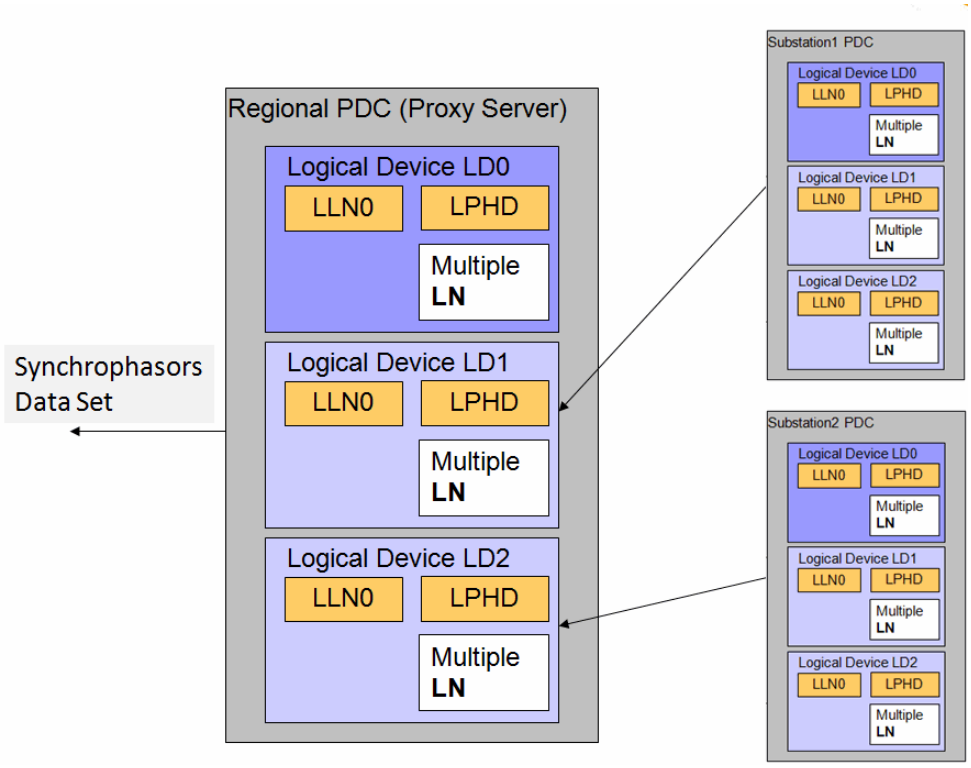

Fig. 4 Regional PDC object model

The Regional PDC model is based on the nesting of logical devices defined in Edition 2 of IEC 61850.

Appendix D. PMU to PDC and PDC to PDC Communications and PDC Testing Recommendations

Smart Grid Synchrophasor Standards and SynchroMetrology Laboratory Support Project

National Institute of Standards and Technology (NIST)

Task 3
Recommendations for
PDC-PMU/PDC-PDC Communications & PDC Testing
For
NIST and NASPI/PSTT

Contract No. SB1341-10-SE-0958

April 2011

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1 Introduction

Title XIII of the 2007 Energy Independence and Security Act (EISA) highlights the components of a secure and reliable power supply, together designated as Smart Grid. To emphasize the importance of Smart Grid as a national priority, through the American Reinvestment and Recovery Act (ARRA), the United States Federal Government has made significant investments in Smart Grid programs. This investment includes providing grants for matching funding for 10 projects related to Synchrophasor technology at the total cost of nearly $400 million dollars. Over 847 PMU will be implemented through these programs with 3 years.

A key to the success of this investment is the availability of Smart Grid interoperability standards that reduce the need for customized integration of new equipment and its associated costs, and ensure that devices deployed today will readily work with devices and systems in the existing grid as well those deployed in the future. EISA (section 1305 of Title XIII) tasks NIST with the development of interoperability standards framework to support Smart Grid.

With the planned proliferation of PMUs, NIST has embarked on several projects to accelerate the harmonization between standards for measuring equipment and communication relevant to measurement of grid conditions by Phasor Measurement Units (PMUs) and standards that cover substation automation, transmitting data from field equipment within the substation and beyond. NIST is also supporting the North American Synchro-Phasor Initiative (NASPI) Performance and Standards Task Team (PSTT) by providing:

- Recommendations for methods for PMU-PDC/PDC-PDC communications as input to the NASPI PSTT
- Recommendations for PDC testing and certification approaches as input to the NASPI PSTT

Through competitive procurement, NIST selected ESTA International, LLC (ESTA), an energy strategy and technology advisory firm and its subcontractor Quanta Technology LLC (QT), an energy technology consulting firm, to support this program.

This document provided recommendation by the ESTA/QT team to NASPI PSTT team for the aforementioned functionality.

1.1 Organization of this Report

This report provides discussion on:

- the issues related to PDC-PDC/PMU-PDC communications and the accompanying ESTA/QT recommendations,
- the issues related to PDC Testing and the accompanying ESTA/QT recommendations the issues related to PDC Testing and the accompanying ESTA/QT recommendations, and
- recommendations for future work related to synchrophasor and PDC standards and guides.

The discussions and recommendations presented in sections 2 and 3 relate to the present work being concluded (approx. May 2011) by NASPI/PSTT subtask teams. These sections provide a brief review of the content of those NASPI/PSTT documents and ESTA/QT's recommendations regarding that content. Section 4 provides additional recommendations for future work by IEEE-PES PSRC working group C4, developing the PDC Guide, and the joint IEEE/IEC working groups working on synchrophasor standards, including IEEE C37.118.2 and IEC 61850-90-5.

-

2 PMU-PDC/ PDC-PDC Communications

2.1 Issues and Recommendations

Communication technology is a key component of any Synchrophasor program. While the merits of Phasor Measurement Units (PMUs) in supporting the operation of the power system have always been apparent since PMUs were introduced in 1988 at Virginia Polytechnic Institute and State University (Virginia Tech), it is the availability of affordable advance communications that is helping the proliferation of PMUs throughout the world.

PMU data can be used both in real-time and recording mode. In the recording mode, information is stored on memory devices and later transferred to other tools and applications for post event analysis. In the real-time mode, information obtained at the PMUs are coordinated and transferred to advanced application programs at the control center via a series of Phasor Data Concentrators (PDCs), hence, the focus on PMU-PDC and PDC-PDC communications.

IEEE C37.118-2005 is the current standard most commonly used for PMU to PDC and PDC to PDC communications. At present, extensive effort is underway to identify and address potential gaps in current standards. These include the efforts in developing IEEE C37.118.1 for Measurement and C37.118.2 for communications aspects of synchrophasors. A driving factor in development of the two standards C37.118.1 and C37.118.2 is the desire for harmonization with IEC standards, namely the report IEC61850-90-5 which focuses on communications aspects. It is envisaged that C37.118.2 and IEC 61850-90-5 will be harmonized and published as dual logo (IEEE and IEC) standards in the future.

In addressing the communications aspects of PMU to PDC and PDC to PDC communications, several issues must be addressed. These issues can be broadly categorized into

- Data Flow Management
  - Data Latency
  - Data Loss
  - Data Quality Indication
- Configuration Management

- Changes in configuration
- Hierarchical configuration

2.2 Data Flow Management

Data management can encounter complications both due to errors in measurements at the source (e.g., incorrect readings, incorrect wiring, incorrect time source etc.) and through errors / delays in the communication network. The focus of this section is the issues related to the communication of such data. Figure 1 below depicts a hypothetical hierarchical configuration containing PMUs, Substation PDC, Transmission Operator PDC, and System Operator PDC

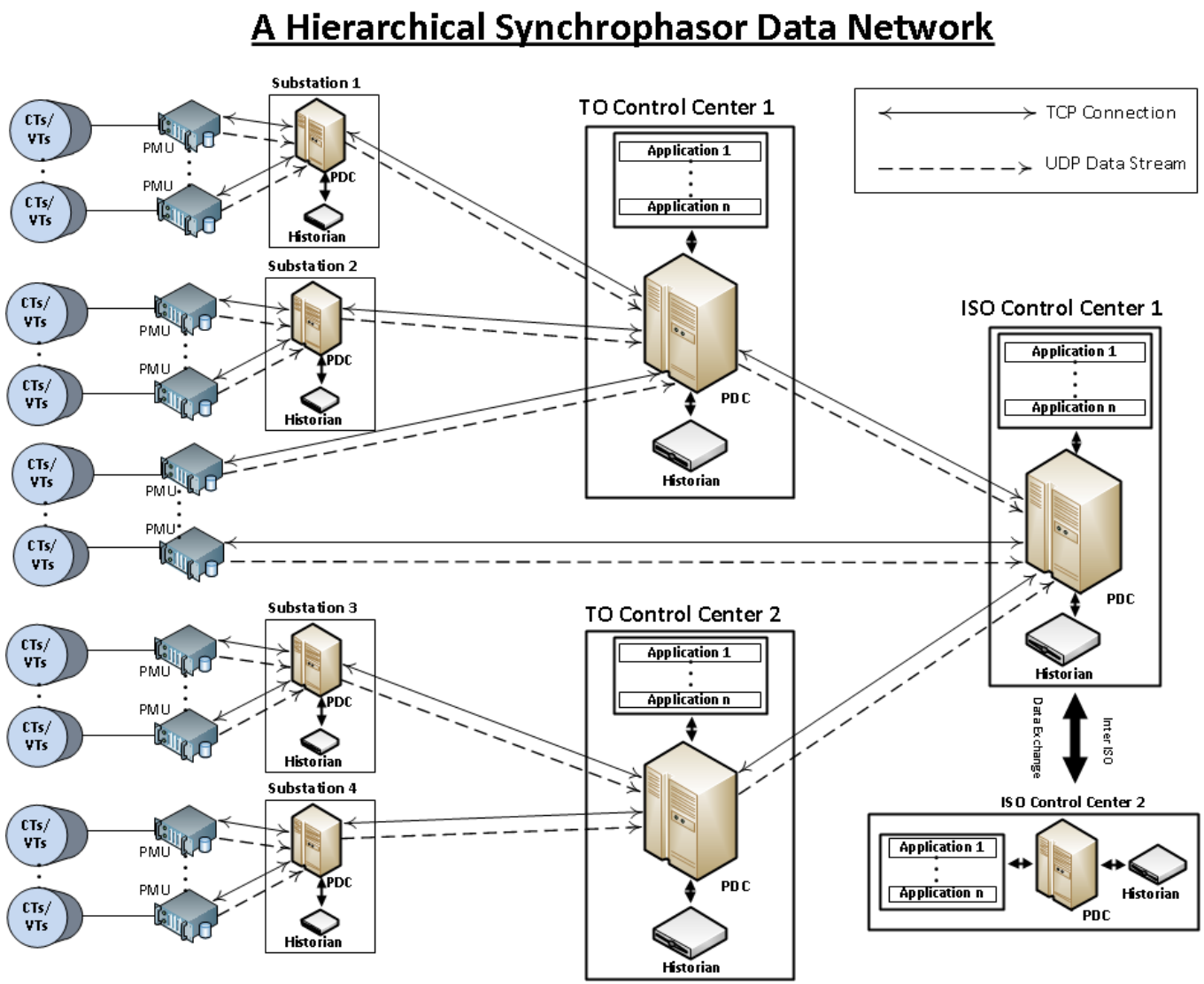

Figure 1: Hierarchical Synchrophasor System Structure

In Figure 1 the PMU data gathered from the CT's and PT's are transferred to the substation PDCs in the substation and further to other PDCs until its final destination. It is important to note that depending on system requirements (e.g., reliability, applications deployed, etc.) the hierarchical architecture can be more complicated and have additional links between various components. Also, not all synchrophasor data may be needed at all control centers; e.g., Transmission Owner (TO) Control Center may require all individual 3-phase system phasors whereas the Independent System Operator (ISO) control centers may only require positive-sequence voltages and currents.

2.2.1 Data Latency

2.2.1.1 Data Latency Issues

In the process shown in Figure 1 it is possible that PMU or PDC data arrives late beyond the wait time of the PDCs (normally 1-4 seconds), while other data, having arrived within the wait time, have already been transmitted.

2.2.1.2 Data Latency Recommendations

To address the above issues regarding data latency, ESTA/QT recommends

- The availability of a protocol to allow sending of data separately.
- Addition of new information to the data message or in the configuration settings to permit interpretation of such separately sent data.

2.2.1.3 Data Latency Recommended Settings

ESTA/QT recommends the following abilities:

- **Wait Time** – The Wait Timer is used to wait for normal data reception. All data received within this time is processed normally (aggregated and sent to destination, dispensed to applications and to the archive).
- **Late Time** – The Late Timer is triggered after Wait Time is over. Any data arriving within this time is accepted as late arriving data. Any data that does not arrive until this timer runs out will trigger the missing data retrieval mechanism. This timer may also take care of wrong order data packets.
- **Retrieval Time** – The Retrieval Timer is triggered after Late Time is over, and data retrieval mechanism is invoked. A response is expected within the Retrieval Time interval, either in the form of the Retrieved Data, or a Lost Data message, indicating that the data is not available. If no response is received, either the mechanism should be invoked again (Retrieval Count times), or if the (Retrieval Count) counter runs out, then an alert is issued. At least a Lost Data message should have been received
- **Retrieval Count** – The Retrieval Count is the number of times a missing data retrieval mechanism is invoked before abandoning the effort and an alert issued. The missing data retrieval mechanism is expected to use a reliable method such as the TCP protocol and normally there should not be a need to use the Retrieval Count to be anything other than one.

2.2.1.4 Data Latency Recommended Quality Features

ESTA/QT recommends the following new features

- **Use Absent Data Tag for absent data** – If data does not arrive until Wait Time is exhausted, the data spot is filled with the Absent Data Tag to maintain data packet integrity.
- **Accept Absent Data Tag in data field** - If a received data value is Absent Data Tag, the receiver should accept it, with the awareness that this means unavailable data at the Source.
- **Data Quality Tag** -Data Quality is to be included with each measured data. The tags include Extrapolated, Interpolated, Computed, Filtered, Sensor Quality, Time Quality, and Test Mode.

2.2.1.5 Retrieve Data Messages

- **Send Retrieved Data packet.** It will include Own ID/Signals ID, Data and time stamp. This mechanism may be triggered for two reasons:
    - If data arrives late at a PDC, and the aggregated data that it should have belonged to has already been sent with Absent Data Tag as substitute value, the device will construct a Retrieved Data packet, including the source ID / signal ID, data and time stamp and send to the Destination over TCP (or by other reliable methods).
    - When a Data Retrieval Request is received from a Destination device and this device has the missing data available to be sent, it is to be sent as Retrieved Data.
- **Accept / decode Retrieved Data packet** A Retrieved Data packet should be accepted and used. This data either came in with an Absent-Data-Tag earlier, or is a result of a Data Retrieval Request.

2.2.2 Lost Data

In the process shown in Figure 1 it is possible that PMU or PDC data sent to another PDC is lost during the transfer.

2.2.2.1 Lost Data Issues

It is possible that data may be lost during transmission. This can be due to an array of events including equipment malfunction, bandwidth issues, misrouting, etc. In this case the Source is unaware that data was not received by the Destination. It may be possible that this data is retained and stored by the Source temporarily. However, currently there is no mechanism for the Destination to retrieve such stored data for possible playback and analytical functions.

2.2.2.2 Lost Data Recommendations

ESTA/QT recommends that new commands and responses to the protocol be provided to allow the Destination to request missing data from the Source and for the Source to send such data, possibly as close to the late data format as possible. The Destination will dispense the data to further destinations. If the Source no longer has the data available, it should be able to send a “no data” message.

ESTA/QT recommends the following new capabilities:

- **Send Data Retrieval Request -** Device ID or Signals ID, Time range - If data has not arrived until the Late Time has run out, the missing data retrieval mechanism should be invoked. A Data Retrieval Request message should be constructed and sent to the source. Data Retrieval Request should result in a response within the Retrieval Time interval. The response may be the missing data itself, or a Lost Data message. In the absence of any response, the mechanism may be invoked Retrieval Count times, then an alert raised.
- **Receive / decode Data Retrieval Request** A Data Retrieval Request should be accepted (and used) from a downstream device.
- **Identify available / not available data** (Some / all Available: Send, Retrieved Data Some / all Unavailable) On receipt of Data Retrieval Request, the device should decode the message and determine if it has the data available. The action to be undertaken depends on the data availability.
    - All requested data available
    - No requested data available
    - Some requested data available.
- **Send Lost Data message** (to include PMU/Signals ID, time stamp(s)) This message is sent for two reasons: 1) if a PMU receives a Data Retrieval Request, and does not have data available, it will send a Lost Data packet to the destination. This will allow all subsequent devices to update their archive, and stop all future Data Retrieval Requests; 2) if an intermediate PDC receives this message from its source device, it should send it to a further destination device.
- **Split Data Retrieval Request for Sources** - If an intermediate PDC device receives a Data Retrieval Request and it does not have the data available for sending, it will split the message into multiple Data Retrieval Request messages for its source devices and send them, in case the data exists there.
- **Accept / decode Lost Data packet** - A Lost Data packet should be accepted (and used) from source devices.
- **Mark archive with Lost Data** - On receipt of Lost Data packet, the archive should be marked so as to stop all future Data Retrieval Requests generation.

2.3 Configuration Management

2.3.1 Change of Configuration

2.3.1.1 Change of Configuration Issues

Currently, addition of a PMU or any modification to an existing PMU such as addition or removal of signals that impacts the contents of the data stream requires a termination of the existing data stream. Its configuration must be changed and data stream restarted. In this process some data, such as the unchanged signals or devices may be lost while the data stream is stopped.

2.3.1.2 Change of Configuration Recommendations

To address the issues identified above, ESTA/QT recommends that new commands/timing be devised for the protocol to communicate the configuration information up and down the data network; allow devices to be ready for change of configuration; allow Sources to change data stream seamlessly, and allow Destinations to latch to the new data stream knowing in advance what the changes would be.

2.3.1.3 Recommended Change of Configuration Command Messages

ESTA/QT Recommends the following new Command Messages

- **Send Device On / Off line** - (to include: Own ID, Data Stream ID, Configuration Delay 1, Change Indication Duration) This command instructs the source device to either go online or offline. It will ask the device to start or stop the specified data stream.
- **Split Device On / Off line command** - The intermediate PDCs need the ability to receive a Device on/off line command from its destination device, and to split it into corresponding Device on/off commands for constituent source devices.
- **New Configuration Command** - (to include: Own ID, Data Stream ID, New Signals ID, Configuration Delay, and Change Indication Duration) - This command instructs the source device to change the content of the data stream. The device should have the ability to generate the command for a source device, and to receive the command from a destination device.
- **Split New Configuration Command** - The intermediate PDCs need the ability to receive a New Configuration Command from a destination device, and to split it into corresponding New Configuration Commands for constituent source devices.

2.3.1.4 Recommended Change of Configuration Information Messages

ESTA/QT recommends the following new information messages

- **New Configuration Information** (to include: Own ID, Data Stream ID, New Signals ID, Configuration Delay 1, and Change Indication Duration) - This message informs a destination device about an imminent change in the contents of the data stream.

- **Aggregate New Configuration Info -**The intermediate PDCs need the ability to aggregate New Configuration Information from corresponding New Configuration Information from its constituent source devices.
- **Current Configuration Information** (to include: Own ID, Data Stream ID, New Signals ID, IP addresses and ports, and Data stream configuration, including TCP/UDP) - This message informs a destination device about the current contents of the data stream. This may be requested by the destination device any time.
- **Request Current Configuration Information** - This message requests a source device for the Current Configuration Info message.
- **Aggregate Current Configuration Information** - The intermediate PDCs need the ability to aggregate Current Configuration Information from corresponding "Current Configuration Information" from its constituent source devices.

2.3.2 Hierarchical Configuration

2.3.2.1 Hierarchical Configurations Issues

Each device (PMUs and PDCs) in the Synchrophasor network needs to be configured separately for Synchrophasor settings such as data formats, data rates, signal content list etc., although they make up one Synchrophasor network. For the proper operation of the Synchrophasor network such settings must be consistent with each other. However, at present there is no method to configure all devices from the control center through a single setup that would ensure consistency and ensure operation.

2.3.2.2 Hierarchical Configuration Recommendation

ESTA/QT recommends that new commands/timings be devised in the protocol to configure the entire network in one setting block. It should also permit intermediate devices to interpret such configuration blocks, split them as appropriate, and send them to further source devices. These commands will permit appropriate acknowledge / compliance / non-compliance etc. messages between devices. These commands would be consistent with the configuration change information / commands recommended in the previous section.

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3 Phasor Data Concentrator Test Requirements Guide

"Synchrophasor measurement data taken at the same sampling instant by various PMUs typically will not arrive at a destination at the same time. This is due to differences in PMU latency and data transmission latency in the communication paths used among all PMUs. Before a real-time application can utilize these data, there is a need to aggregate, validate and time-align the received data. This set of operations is done by a phasor data concentration [PDC] function."[4]

With the proliferation of Phasor Data Concentrators as an important element of Synchrophasor schemas NASPI PSTT has embarked on development of a PDC Guide, including a PDC testing guide for the industry. Many industry practitioners are actively involved with the program reflecting the high level of interest. Active participation of several stakeholders with varied perspectives has resulted in a rich array of requirements with varying order of priority for some of these requirements, much like development of other industry standards. To meet its objectives, NASPI PSTT has instituted an accelerated timeline. NIST, in support of NASPI PSTT has retained ESTA International and its subcontractor Quanta Technology (ESTA/QT) to provide recommendations to NASPI PSTT for the PDC Test Guide.

ESTA/QT recommends that PDC Testing be focused on the "core" PDC functional requirements as outlined in the NASPI PSTT draft PDC functional Specification. These include basic communication tests (as specified in section 2 above) and the following:

- Format conversion – capability of receiving real-time synchrophasor data streams from PMUs and other PDCs in various protocols and formats, and at various rates and the capability to convert into a common format.
- Coordinate conversion – capability to process and/or convert data both in Cartesian and Polar coordinates and in fixed integer and floating point formats.
- Wait Time and Latency calculation - capability to allow maximum wait time for data arriving from a PMU or another PDC, and to measure/track overall PDC latency. Wait time may be set up in absolute time reference (relative to a GPS synchronized time) or relative time reference (relative to the arrival time of the first PMU data with the relevant time tag).
- Data Alignment – capability to align PMU and PDC data according to their time tags (as opposed to time of arrival).
- Data re-sampling – capability to provide data re-sampling (both down re-sampling and up re-sampling functionality) with clear requirements for anti-aliasing filtering and statement of the impact of re-sampling on accuracy.
- Data Validation – capability to provide data validation in accordance with the prevailing standard and/or (optionally) advanced model-based data validation applications.

[4] Source: North American SynchroPhasor Initiative (NASPI), Performance & Standards Task Team (PSTT), Draft – Phasor Data Concentrator Functional and Performance Requirements, Updated: April 2011

- Internal buffering – capability to retain and store data for up to a predefined time period to prevent data losses while communication to other PDCs or applications is unavailable.
- Configuration validation – capability to auto reconfigure in case of configuration changes
- Phase and amplitude adjustment – capability to make calibration and bulk-type adjustments to both phasor amplitude and phase.

Naturally, if PDCs have additional functionalities, tests should be devised to verify adequate performance of those functionalities; nevertheless, the industry "PDC test guide" should be focused on those key functions that all (or most) phasor data concentrators should have. Additional common functions that many PDCs have, but are not necessarily part of every PDC are:

- Data Storage and Retrieval Function
- PMU/PDC Performance Monitoring Function
- Event Detection Function
- Phasor Data Gateway Function
- Synchrophasor System Latency Measurements

Even though the above functions are very valuable, they are not necessarily part of every PDC; consequently, the detailed requirements of each of these functionalities should be optional in the PDC guide, and in turn, these functions should not be the focus of the PDC test guide. Rather, the core PDC functions provided earlier above should be the focus of the test guide.

The tests to be performed on PDCs can be divided into several categories. These include:

- Design tests – These tests focus on verifying all core features of a specific PDC against its functional specifications including applicable industry standards.
- Type tests – Type tests are typically a subset of design tests. These tests focus on select core PDC functionality and verify PDC performance for such selected functionalities.
- Application tests - These tests are designed to verify the performance of the PDC when supporting applications using the Synchrophasor data.
- Interoperability tests – These tests focus on the ability of the PDC to interoperate with other devices within the Synchrophasor network.
- Commissioning tests – These tests verify proper installation and operation of the PDC.
- Cyber security tests – These tests verify conformance to prevailing cyber security policies such as NERC CIP and NISTIR 7628.

There are several different types of PDCs, serving different applications/functions. Even though the PDC Testing Guide should focus on core PDC requirements, it should also encourage the users to develop a

specific test plan based on the applications/functions of interest (now and in the foreseeable future) being served by the PDC.

It is recommended that PSTT provide these recommendations and the related PSTT documents (PDC Testing Guide and PDC Functional Requirements Document) to IEEE PSRC WG C4 being formalized in May 2011 and work with PSRC to further develop the PDC Guide into an official IEEE document.

ESTA/QT recommends that PSTT coordinate with projects that have synchrophasor system testing (especially SGIG synchrophasor projects) to validate the content of the PDC Testing Guide (and PDC Functional Requirements Document) and revise the guide. Also, consider performing more plug-fests at NASPI-PSTT, showing PDC testing and interoperability. Perhaps the October 2011 NASPI meeting would be an excellent venue to show and validate some of the PDC and interoperability tests.

ESTA/QT recommends that various synchrophasor communication requirements and details captured in IEC 61850-90-5 in the coming months be reviewed and PSRC C4 working group should consider developing or modifying PDC tests to allow testing for features introduced in IEC 61850-90-5.

Any generic PDC hardware testing (such as ElectroMagnetic Compatibility [EMC] tests) will be a function of the environment where the hardware will be used and should be governed by the typical requirements of the user (e.g., power company) for other devices deployed in similar environment. The PDC Testing Guide should focus on testing for data concentration function only and not EMC tests.

4 Summary and Recommendations for Future Work

The working groups within NASPI PSTT (i.e., Subtask teams – which includes participants from QT) have made great progress in the past 6 months in developing documents, requirements, and guidelines for various aspects of synchrophasor systems, including synchrophasor communications, phasor data concentration functions, and testing. The documents developed will address many gaps in the present synchrophasor system projects and interoperability challenges. These documents contain, nevertheless, mostly consensus-based requirements. With synchrophasor technology deployment and solutions being in an early stage, infancy if we may, naturally, the technology is going through significant growth, and the balance between setting rigid interoperability standards and allowing creative product development and enhancements is a very challenging one. We believe the NASPI/PSTT subtask teams are on the right path in keeping this balance. The material produced by the subtask teams will go through more refinements and evolution as they go through the IEEE standardization process in the next few months. More specifically, in addition to the recommendations given in previous sections, we have the following recommendations for further enhancement of these requirements, guidelines, and standards:

- Use of Multicast UDP communication for synchrophasor data streaming should be the preferred mode (minimum requirement) for synchrophasor data communications. We recommend addressing this in both IEEE C37.118.2 and in IEC 61850-90-5. Use of multicast

UDP communication can address the low latency required for certain synchrophasor applications (e.g., closed-loop control applications) while keeping the data communication bandwidth/capacity requirements to a minimum.

- Communicating config file information and commands in TCP/IP and streaming synchrophasor data in UDP/IP (multicast), should be preferred (minimum requirement) for synchrophasor data communication; accordingly, method(s) of initiating UDP streaming via TCP command should be standardized. TCP/IP provides high reliability (through communication handshake) for messages reaching destinations at the expense of more latency and possibly backing up the network with too much traffic during temporary communication breakdowns. Accordingly, TCP/IP is ideal for non-time-critical data that would require "guaranteed" delivery, such as configuration information and commands. UDP communication is more efficient (with respect to using communication bandwidth) and provides more consistent (and shorter) latency and, therefore, is more suitable for continuous real-time streams, e.g., synchrophasor measurement data.
- The guides produced by PSTT/NASPI subtask teams include several "protocol independent" solutions to the gaps in present synchrophasor standards. IEEE and IEC working groups should consider "protocol-specific" implementations of these solutions in the corresponding standards (mostly IEEE C37.118.1 and C37.118.2 and IEC 61850-90-5).
- Basic educational details about IP (Internet Protocol) communication technology should not be included in synchrophasor standards/guides; rather, they can be used by reference. Presently, the NASPI/PSTT document "Guide on PMU-PDC and PDC-PDC Communication" contains too much detail on basic IP communications. . The focus of the guide should be on truly new parts of the synchrophasor technology. Even though the basic details of IP technology may be new for some power engineers (and have educational value), they are not new to the informational technology (IT) professionals who will be involved in developing/deploying communication systems for synchrophasor systems. Accordingly, having so much trivial details in this guide may confuse the users and will detract from the key points of the guide. Those interested can find IP technology information in a multitude of textbooks and established publications/courses.
- To date, the focus of the PDC Requirements Document and the PDC Test Guide has been appropriately on "core PDC functions." Perhaps, some non-core functions that are of high interest should also be standardized in more details, e.g., storage/historians having data arrival time-stamp. We recommend PSRC WG C4 developing the IEEE Guide for PDCs (PC37.244) to take this into consideration. There is always a balance between the efficiency of working with simple functions and the flexibility that complex systems can provide. As a starting point, appropriately, NASPI/PSTT team focused on critical/core functions first. As the industry matures, more complex functions can be addressed through standardization

A Appendix - Table of Contents of Industry Documents

A.1 Guide on PMU-PDC and PDC-PDC Communications

This guide is under review and not approved as of this report date. The table of contents below is for Rev 3.; last updated on March 30, 2011.

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A.2 Phasor Data Concentrator Test Requirements Guide

As of this reporting date, the Phasor Data Concentrator Test Requirement Guide has been provided to NASPI PSTT for review and approval. Below is the table of contents as of April 1, 2011.

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